REMARKS

The application has been carefully reviewed in light of the Office Action dated May 21, 2003. Claims 1, 24 and 25 have been amended. Claims 1-25 are pending in this case.

Claims 1-25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lepejian (U.S. Patent No. 6,154,714) in view of Okubo et al. (U.S. Patent No. 5,872,862). Applicants respectfully traverse the rejection and request reconsideration.

Claim 1 recites a semiconductor inspection system comprising a navigation system for storing design information such as CAD data of a semiconductor chip and for setting capturing and inspecting conditions including a region on a semiconductor wafer subject to inspection based on the design information. Also included is a scanning electron microscope system for performing actual capturing of the semiconductor wafer and for executing inspection in accordance with the capturing and inspecting conditions being set. The navigation system sets a template based on the design information, and performs a matching process whereby the template that is registered in advance is matched with a pattern within an image provided by the scanning electron microscope, wherein a portion of the image provided by the scanning electron microscope that corresponds to the template is re-registered as a template for the pattern matching process.

The method of Lepejian fails to teach or suggest the limitations of claim 1. Lepejian discloses a method for testing an integrated circuit wafer by defining a plurality of dice where at least one die has at least one known defect. The method of Lepejian selects for testing a first die having a known defect whereby connectivity and defect information is analyzed to determine a probability of failure for each known defect on the first die. A sequence of tests is modified based on the information in order to ensure that at least one test that directly relates to a known defect is performed prior to performing tests that are unrelated to a defect.

The method of Lepejian fails to teach or suggest a semiconductor inspection system that acquires information for the creation of a template for the pattern matching process. For example, Lepejian attempts to reduce the cost of testing by giving priority to the measurement of a die or the like with higher probabilities of failure, or by rejecting fatal defects by assigning weights to such defects.

The object of the present invention is to provide a semiconductor inspection system in which a high-correlation value and stable matching process can be performed between a template based on design data and an SEM image. For this purpose, a template is created based on design information, and a position in an image provided by the scanning electron microscope is detected by pattern matching using the template that corresponds to the template. A portion of the image provided by the scanning electron microscope that corresponds to the detected position is then re-registered as a template for the pattern matching process.

An actual SEM image has a high correlation value with respect to an SEM image as an object of measurement and is therefore suitable for pattern matching. The present invention sets an SEM image based on the matching process in light of design data. The resultant SEM image detected by the matching process is used as a template for matching. Thus, an operator free setting for template making is created that is not addressed by Lepejian.

In addition, Lepejian fails to teach or suggest a semiconductor inspection system in which there is a re-registering of an image portion provided by the scanning electron microscope that corresponds to the detected position as a template for the pattern matching process. Therefore, claim 1 is allowable over Lepejian.

Okubo discloses an electron beam tester that scans a sample with an electron beam to provide a secondary electron image, which is used to match wiring patterns of the secondary electron image with wiring patterns produced from CAD data. This process

measures the voltages of the wiring patterns and corrects deformation of the secondary electron image.

Okubo fails to teach or suggest all of the limitations of claim 1. For example, Okubo fails to teach or suggest a portion of the image provided by the scanning electron microscope that corresponds to the detected position being re-registered as a template for the pattern matching process. To the contrary, Okubo merely discloses the matching between CAD data and a SEM image. Okubo also fails to teach or suggest re-registering an image portion provided by the scanning electron microscope that corresponds to the detected position as a template for the pattern matching process. Therefore claim 1 is allowable over Okubo.

Thus, the proposed combination does not teach or suggest the invention as claimed. The combination of Lepejian and Okubo does not teach or suggest all of the limitations of claim 1. Therefore, the rejection of claim 1 under 35 U.S.C. § 103(a) should be withdrawn.

Claims 2-23 depend from claim 1 and are allowable over the combination of Lepejian and Okubo for the reasons mentioned above with respect to claim 1, and also because Lepejian and Okubo fail to teach or suggest the respective inventive combinations defined by claims 2-23.

Claim 24 recites a semiconductor inspection method whose steps include *inter alia* re-registering an image portion provided by the scanning electron microscope that corresponds to the detected position as a template for the pattern matching process. Claim 25 recites a similar limitation to that of claim 24, re-registering as a template a portion of an image provided by an electron microscope that is detected by the matching process.

For the reasons mentioned above with respect to claim 1 concerning re-registering an image portion provided by an electron microscope, Lepejian and Okubo fail

to teach or suggest the limitations of clam 24 and 25. Therefore, the rejection of claims 24 and 25 under 35 U.S.C. § 103(a) should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: October 8, 2003

Respectfully submitted,

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